In the Claims:

1. (Previously Presented) A semiconductor chip comprising:

a semiconductor substrate comprising an active region;

a first structure formed on the active region, the first structure being fully silicided; and

at least one dummy silicide structure formed on the semiconductor substrate.

2. (Original) The semiconductor chip of claim 1 wherein the first structure is a transistor gate electrode of a transistor.

3. (Original) The semiconductor chip of claim 2 wherein the transistor further comprises a gate dielectric underlying the first structure, the gate dielectric comprising a high permittivity dielectric selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthalum oxide, cerium oxide, titanium oxide, and tantalum oxide.

4. (Original) The semiconductor chip of claim 1 wherein the dummy silicide structure is located in the active region.

5. (Original) The semiconductor chip of claim 1 wherein the dummy silicide structure is located in an isolation region separate from the active region.

6. (Original) The semiconductor chip of claim 1 wherein the first structure and dummy silicide structure each comprises nickel silicide.

7. (Original) The semiconductor chip of claim 1 wherein the first structure and dummy silicide structure each comprises a silicide of a material selected from the group consisting of nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium, zirconium, and platinum.

8. (Original) The semiconductor chip of claim 1 wherein the first structure and dummy silicide structure each comprises germanium.

9. (Original) The semiconductor chip of claim 1 wherein the semiconductor substrate is a silicon substrate.

10. (Original) The semiconductor chip of claim 1 whercin the semiconductor substrate is a semiconductor-on-insulator substrate.

11. (Original) The semiconductor chip of claim 1 further comprising a contact etch-stop layer overlying portions of the first structure.

12. (Original) The semiconductor chip of claim 1 further comprising a dielectric layer overlying the first structure and dummy silicide structure.

13. (Previously Presented) An integrated circuit chip comprising:

a substrate having an active region and an isolation region;

a transistor formed on the active region, the transistor having a source region, a drain region, and a fully silicided gate electrode; and

at least one dummy silicide structure formed on the substrate.

14. (Original) The integrated circuit chip of claim 13 wherein electrical contacts are electrically coupled to the source region, the drain region, and the fully silicided gate electrodes.

15. (Original) The integrated circuit chip of claim 13 wherein the dummy silicided structure is located in the active region.

16. (Original) The integrated circuit chip of claim 13 wherein the dummy silicided structure is located in the isolation region.

17. (Original) The integrated circuit chip of claim 13 wherein the fully silicided gate electrode and dummy silicided structure comprise nickel silicide.

18. (Original) The integrated circuit chip of claim 13 wherein the fully silicided gate electrode and dummy silicided structure comprise a silicide of a material selected from the group consisting of nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium, zirconium, and platinum.

19. (Original) The integrated circuit chip of claim 13 wherein the fully silicided gate electrode and dummy silicided structure comprise germanium.

20-43. Canceled